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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/542,211	03/16/2006	Frank J. Juskey	102441-209	1746

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WIGGIN AND DANA LLP
ATTENTION: PATENT DOCKETING
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EXAMINER	
CLARK, JASMINE JHIHAN B	
ART UNIT	PAPER NUMBER
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/542,211	JUSKEY ET AL.	
	Examiner	Art Unit	
	Jasmine J. Clark	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,4,6-10,12 and 14-18 is/are rejected.

7)☒ Claim(s) 3,5,11 and 13 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ~~4/5/06~~ 7/14/5
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Information Disclosure Statement

1. The IDS filed 4/7/6 has been considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1, 2, 4, 6-10, 12, 14-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Lyu et al. (US 6,849,949 B1).

Lyu '949 shows a structure of a semiconductor device, comprising a plurality of die package 170 for example (see Fig. 16), each including: a lead frame 121 having a plurality leads having a first surface and a down set portion extending from the first surface; a semiconductor die 110 disposed in the central region and electrically connected to the lead, the semiconductor die 110 having a first surface formed thereon,

the first surface of the semiconductor die 110 being substantially coplanar with the first surface formed on each of the leads, and an encapsulant eg., 150 disposed in the central region and covering the semiconductor die and a portion of the leads, the first surface of the leads and the first surface of the die 110 being exposed from the encapsulant, and the first surface of the semiconductor die 110 and the down set portions of the leads 121 forming a cavity; wherein the plurality of die package are stacked such that at least a portion of the encapsulant 150 is disposed in the cavity of a next higher die package in the stack; and wherein the plurality of leads are disposed on eg., two sides of the central region (claim 8), please see Fig. 16, eg.

Concerning claims 4 and 6, wherein the lower surface of the down set portion of at least one die package in the stacked is soldered to the upper surfaces of the down set portions of an adjacent die package in the stack, please see column 7, line 31 for a solder.

Initially, and with respect to claim 6 "wherein the package in the stack are adhere together prior to being soldered", note that a "product by process" claim is directed to the product per se, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the Applicants have burden of proof in such cases as the above case law makes clear.

Concerning claim 7, wherein the sides of the encapsulant 159 are tapered, please see column 5, lines 50+.

Concerning claims 9, 10, 12, 16, and 17, Lyu '949 discloses a method for forming a semiconductor die assembly, the method comprising:

Forming a plurality of individual semiconductor packages (see Figs. 2 and 3 or Figs. 14 and 15) including: providing a lead frame 21 having a plurality of leads surrounding a central region, each of the leads including a first surface formed thereon, disposing a semiconductor die eg., 110 in the central region, the semiconductor die 110 having a first surface formed thereon, the first surface of the semiconductor die being substantially coplanar with the first surface formed on each of the leads, electrically connecting the semiconductor die 110 to the leads, covering a portion of the semiconductor die and a portion of the leads with an encapsulant 150, and shaping each of the leads (see Fig. 14 eg.,) to include a first surface and a down set portion extending from the first surface, the first surface of the leads and the first surface of the semiconductor die being exposed from the encapsulant 150, and the first surface of the semiconductor die 110 and the down set portions of the leads forming a cavity;

Stacking the plurality of individual semiconductor die package such that at least a portion of the encapsulant is disposed in the cavity of a next higher semiconductor die package in the stack; and

Electrically interconnecting corresponding leads of the stacked semiconductor die packages.

Concerning claims 10, 12, 16 and 17, please see the above discussion under claims 2, 4, 7 and 8, eg..,

Concerning claims 14, 15, and 18, the method of claim 12, further comprising, dipping the leads in a solder bath; adhering the semiconductor packages in the stack together prior to dipping; and adhering the semiconductor die packages in the stack together prior to electrically interconnecting, please see column 7, lines 18+.

3. Claims 3, 5, 11, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The applied reference '949 does not literally disclose wherein the leads of each semiconductor die package in the stack are of equal length; and wherein solder balls are attached to the down set portions of the packages.

References Cited

4. The references are cited and should be carefully considered: Isaak (US 6,180,881 B1), Fee et al. (US 6,876,066 B2), Shin et al. (US 6,982,488 B2), and Hinrichsmeyer et al. (US 4,996,587) show a semiconductor die stack and method of making.

Telephone Inquiry Contacts

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine J. Clark whose telephone number is (571) 272-1726. The examiner can normally be reached on Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jjbc/1/22/7

JASMINE CLARK
PRIMARY EXAMINER